

- I Recommended for use with ADSL Chipset in customer premise applications.
- I Operating temperature range:: -10°C to+60°C.
- I Storage temperature range: -25°C to +75°C.
- I RoHS compliant

**Electrical Specifications @ 25°C**

Part Number	Turns Ratio (±5%)	OCL (μH ±5%) @ 10KHz/0.1 V		DC Resistance (Ω Max)				Leakage Inductance (μH Max)	Isolation Voltage (Vrms)	
		1-4	1-5	8-10	7-9	1-3	2-4		PRI/SEC	CORE
ACK4A1TA	8-10:7-9:1-3:2-4	1-4		8-10	7-9	1-3	2-4	1-4	1500	
	1:1	470		1.09	1.47	1.28	1.25	13		
ACA4BASB	10-6:1-5	10-6	1-5	10-7	9-6	1-4	2-5	10-6	1500	
	3.3:1	800	74	0.8	0.8	0.25	0.25	15		
ACK4A1TC	1-3:2-4:7-9:8-10	1-4		7-9	8-10	1-3	2-4	1-4	1875	
	1:1:1:	440		0.48	0.48	0.59	0.59	12		
ACA4B1YC	1-3:2-4:9-7:10-8	1-4		1-3	9-7	10-8	2-4	1-4	1650	
	1:1:1.1:1	2000		0.65	0.65	0.65	1	10		
ACA4B1XC	1-3:2-4:9-7:10-8	1-4		1-3	2-4	9-7	10-8	1-4	1650	
	1:1:1.1:1	1200		0.75	1	1	1	10		
ACK4C2TD	1-5:10-6	10-6		1-4	2-5	9-6	10-7	10-6	PRI/SEC	CORE
	2:1	410		0.4	0.4	0.2	0.2	10	2000	1500
ACA4B2RD	1-4:2-5:9-6:10-7	10-6		1-4	2-5	9-6	10-7	10-6	1650	
	1:1:2:2	100		0.3	0.3	0.55	0.55	12		
ACK4C1YC	1-4:10-7	10-7		1-3	2-4	10-8	9-7	10-7	1875	
	1:1	5000		0.85	1.15	1	1	12		
ACK3ABQE	1-4:8-5	1-4		1-3	2-4	8-6	7-5	1-4	1875	
	1.9:1	92.5		0.275	0.275	0.135	0.135	15		
ACK2A1RE	1-4:8-5	1-4		1-3	2-4	8-6	7-5	1-4	1875	
	1:1	100		1.1	1.1	0.86	0.86	7		

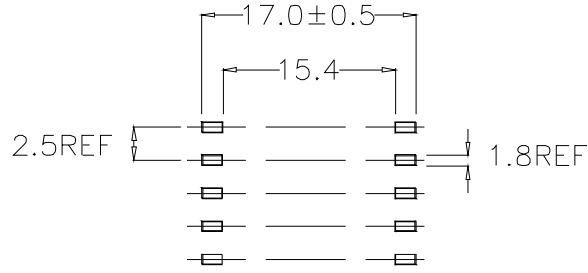
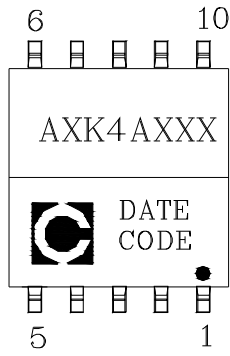
**NOTE:**

1. Explanation of 2<sup>nd</sup> letter of P/N (Part Number)

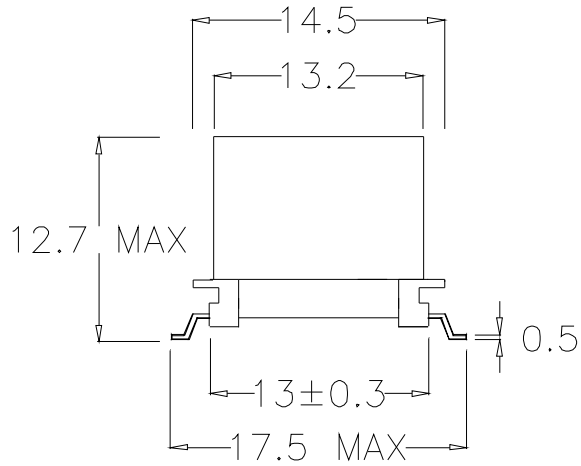
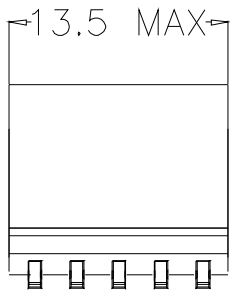
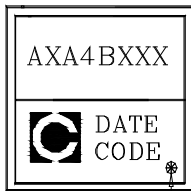
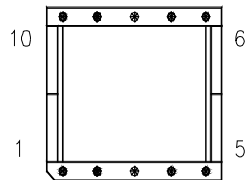
R	External terminals lead free
C	Whole part RoHS and lead free

2. Explanation of 4<sup>th</sup> and 5<sup>th</sup> letters of P/N (Part Number) : Package Type

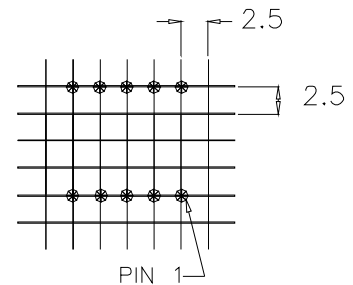
**Mechanicals**

**4A**


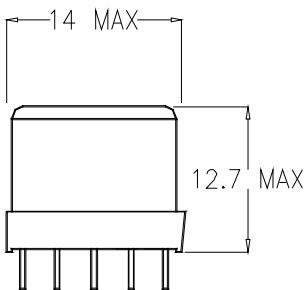
SUGGESTED PCB PAD LAYOUT


**4B**

 DOT INDICATES PIN# 1  
TOP VIEW


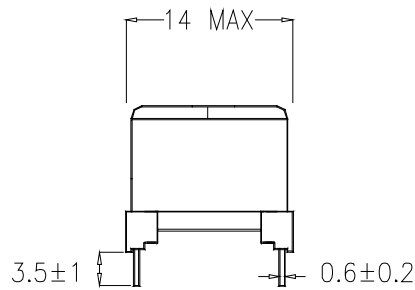
BOTTOM VIEW

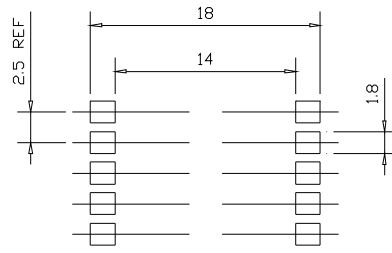
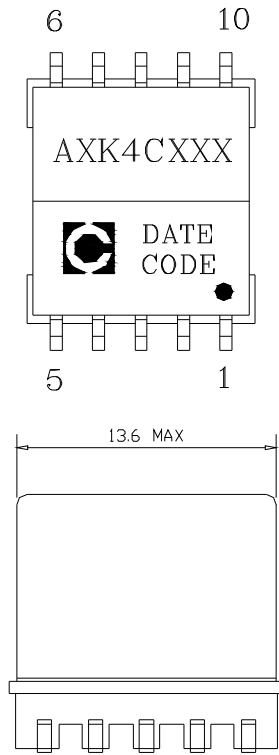
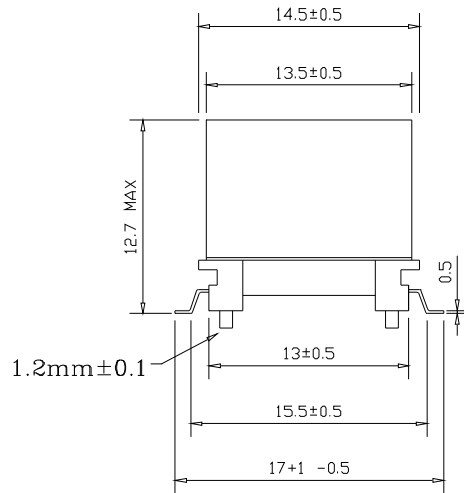
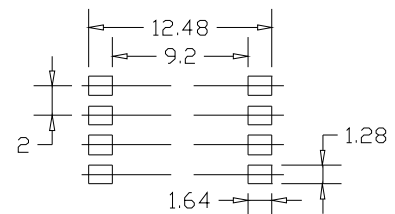
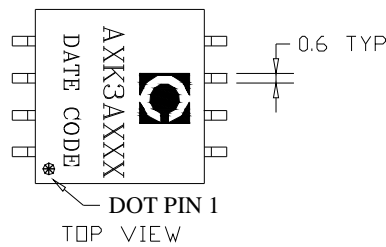
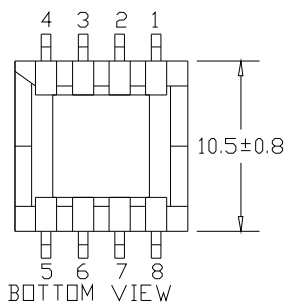
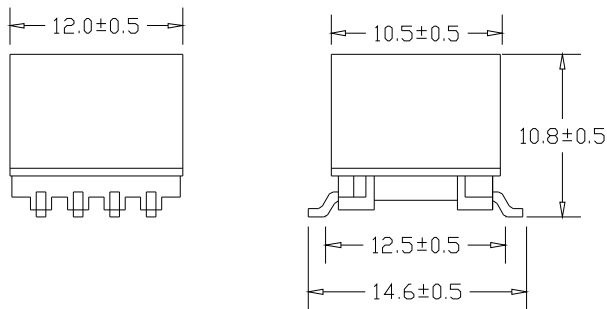


SUGGESTED LAND PATTERN

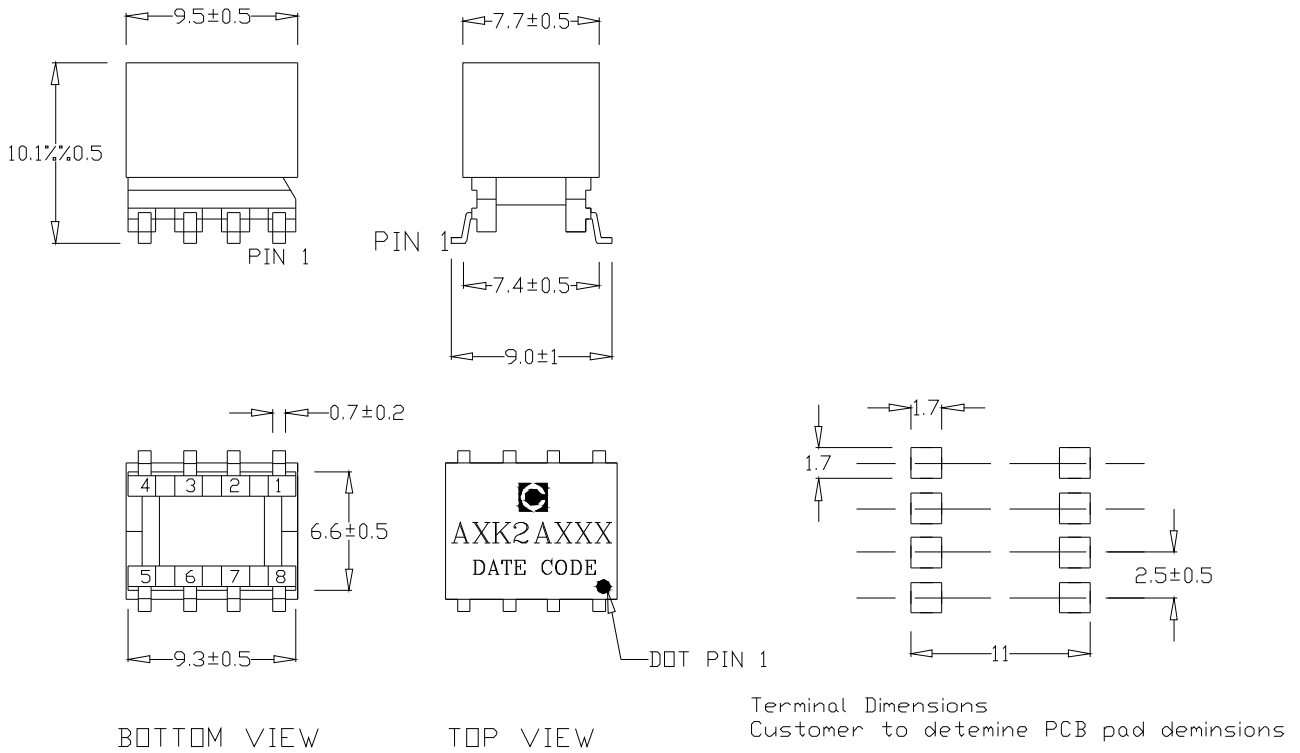


PIN 1



**4C**

**SUGGESTED PCB PAD LAYOUT**

**3A**

**SUGGESTED PCB PAD LAYOUT**

2A



## Schematics

